REMARKS

Claims 1-8 and 20-21 are pending. By this Amendment, claims 1 and 20-21 are amended to clarify the claimed subject matter, and claims 22-23 are canceled. Further, the specification has been amended to correct minor typographical errors. Support for these amendments is provided in the specification at least at page 9, lines 17-22, page 10, lines 8-20 and Figs. 1-3. No new matter has been added. Reconsideration in view of the above amendments and following remarks is respectfully requested. The attached Appendix includes marked-up copies of each rewritten paragraph (37 C.F.R. §1.121(b)(1)(iii)) and claim (37 C.F.R. §1.121(c)(1)(ii)).

I. OBJECTIONS TO THE SPECIFICATION

The Office Action objects to the specification and asserts that there is no support for the claimed terminology "a semiconductor having a channel region and at least one portion standing outside of the channel region in a gate-width direction perpendicular to a gate length direction that is a direction in which one of the plurality of data lines extends" and "the at least one portion and at least one of a source region and a drain region being separated by an extension of the gate electrode and the extension extending in the gate length direction outside of the semiconductor region." Claim 1 has been amended for clarification. Support for the subject matter in claim 1 is provided throughout the specification, and at least at page 9, lines 17-22, page 10, lines 8-20 and Figs. 1-3. See also the explanation under section II. Withdrawal of the objection to the specification is specifically requested.

II. THE DRAWINGS SATISFY ALL FORMAL REQUIREMENTS

The Office Action objects to the drawings and asserts that the drawings do not show the at least one portion and at least one of a source region and a drain region being separated by an extension of the gate electrode. Claims 1 and 20-21 have been amended for clarification. Further, Fig. 3 shows at least one portion (the semiconductor layer 1a that

extends adjacent to contact hole 7) and at least one of a source region (adjacent contact hole 5; see also page 9, lines 17-18) and (a drain region, i.e., the region adjacent contact hole 8 in Fig. 2; see also page 9, lines 18-20) being separated by an extension of the gate electrode (see Fig. 3), the gate electrode being extended to an area adjacent contact hole 7; see page 10, lines 16-20 of the specification. Thus, withdrawal of this objection to the drawings is specifically requested.

III. CLAIMS 1-8 AND 20-23 SATISFY THE REQUIREMENTS OF 35 U.S.C. §112, FIRST PARAGRAPH

The Office Action rejects claims 1-8 and 20-23 under 35 U.S.C. §112, first paragraph. This rejection is moot as to claims 22-23 which have been canceled. The Office Action asserts that it is not clear where support for "the at least one portion and at least one of a source region and a drain region being separated by an extension of the gate electrode" is found in the specification. Claim 1 has been amended for clarification. Based on the discussion under Section II of this Amendment, withdrawal of this rejection is respectfully requested.

IV. THE CLAIMS DEFINE PATENTABLE SUBJECT MATTER

The Office Action rejects claims 1, 3-7 and 21-23 under 35 U.S.C. §102(b) over U.S. Patent 5,614,730 to Nakazawa et al.; claim 2 under 35 U.S.C. §103(a) over Nakazawa et al. in view of U.S. Patent 5,316,960 to Watanabe et al.; claim 8 under 35 U.S.C. §103(a) over Nakazawa et al; and claim 20 under 35 U.S.C. §103(a) over Nakazawa et al. and further in view of JP 06163891 to Nishihara et al. Applicant respectfully traverses these rejections

In particular, Applicant asserts that neither Nakazawa or Nishihara, alone or in combination, teach, suggest, or render an electro-optical device including a plurality of transistors having a gate electrode and a semiconductor layer, wherein the semiconductor layers comprises a source region that is connected to the pixel electrode through a contact hole, a drain region that is connected to the data line through a contact hole, a channel region

disposed under the gate electrode, and the channel region having a semiconductor portion protruding out of the channel region and not being covered with the gate electrode, as recited in claim 1.

The Office Action (at page 4, lines 6-10) provide that Nakazawa discloses in Figs. 19A-19C and 20 a semiconductor layer 102 having a channel region and at least one portion extending outside of the channel region in a gate-width direction perpendicular to a gate-length direction that is a direction in which one of the plurality of data lines extends. The "channel region" of Nakawzawa extends perpendicular to a direction in which the plurality of data lines 108 extend, and not along (or parallel to) a direction in which one of the plurality of data lines extends, as recited in claim 1. See, e.g., Fig. 19A of Nakazawa.

Claim 1 discloses the semiconductor layer including at least three parts. That is, a first part having a source region on the bottom side of the semiconductor having a contact hole 5. See, e.g., Figs. 2 and 9 of the application. A second part is disclosed as having a drain region, shown at the upper and right side of the semiconductor layer having a contact hole 8, and a third part is disposed under the gate electrode. The third part has a portion protruding out of the gate electrode (channel region in the semiconductor layer).

Nakazawa discloses a first part (source) and a second part (drain). However, Nakazawa fails to teach or suggest a third part having a semiconductor portion that protrudes out of the gate electrode. As shown in Fig. 19A of Nakazawa, the right part (drain) of the semiconductor layer 102 has a contact hole 1905 corresponding to the second part, and the left part (source) of the semiconductor layer 102 has a contact hole 1906 corresponding to the first part. However, Nakazawa fails to teach or suggest that the third part (with contact hole 1904) having a portion protruding out of the gate electrode, as recited in independent claim 1.

Furthermore, Nakazawa also discloses that the semiconductor layer 102 is located only at the region located adjacent to the gate electrode 103. However, Nakazawa fails to

teach or suggest a semiconductor portion protruding out of the channel region and not being covered with the gate electrode, as recited in independent claim 1. To the contrary, Nakazawa only teaches what is known conventionally (see the specification at col. 10, lines 14-16), i.e., that the semiconductor layer 102 does not extend toward the outside of the channel region of the semiconductor layer 1a. See, e.g., fig. 19A of Nakazawa. In Fig. 19a of Nakazawa, only the end of the gate electrode 103 extends outside of the channel region, and not the semiconductor region 102 that forms the transistor.

Nishihara fails to make up for the deficiencies of Nakazawa disclosed above. In particular, Nishihara discloses in Figs. 7 and 8 portions of a scanning line 5 that form a gate electrode. In stark contrast to Applicant's claimed invention, Nishihara discloses that the lower end in the gate-length direction of the gate electrode 103 fails to teach or suggest a semiconductor portion protruding out of the channel region and not being covered with the gate electrode, as recited in claim 1.

Wantanabe also fails to make up for the deficiencies of Nakazawa and Nishihara, discussed above either alone or in combination.

For at least these reasons, the applied references fail to teach, suggest, or render each and every feature as the claimed invention. Thus, Applicant asserts that independent claim 1 defines patentable subject matter. Claims 2-8 and 20 depend from the independent claim 1, and therefore also define patentable subject matter. Accordingly, Applicant respectfully request that the rejections under 35 U.S.C. §102(b) and 35 U.S.C. §103(a) be withdrawn.

V. CONCLUSION

In view of the foregoing, Applicant respectfully submits that this application is in condition for allowance. Favorable consideration and prompt allowance are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact Applicant's undersigned representative at the telephone number set forth below.

Respectfully submitted,

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JAO:RZE/dmw

Date: January 31, 2003

Attachment:
Appendix

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry;
Charge any fee due to our Deposit Account No. 15-0461

APPENDIX

Changes to Specification:

Page 10, lines 8-20:

Fig. 3 is an expanded plan view of the TFT shown in Fig. 2. In Fig. 3, the gate-length direction is a direction in which the data line 6a extends, and the gate-width direction is a direction perpendicular to the gate-length direction. Each semiconductor layer 1a is electrically separated completely from the other semiconductor layers by a mesa-etching method, LOCOS method, or the like. The gate electrode 3 is provided on the semiconductor layer 1a through an insulating film. At least one portion of the ends in the gate-width direction of each gate electrode 3 is disposed on the semiconductor layer 1a, which does not extend toward the outside of the channel region of the semiconductor layer 1a, as in a conventional TFT. The ends in the gate-length direction of the gate electrode 3 extend toward the outside of the channel region of the semiconductor layer 1a. A contact hole 7 for connection to the capacitance line 3b is provided on at least one of the ends of the semiconductor layer 1a extending toward the outside of the gate electrode 3.

Changes to Claims:

Claims 22-23 are canceled.

The following is a marked-up version of the amended claims:

1. (Twice Amended) An electro-optical device, comprising:

a substrate;

a pixel electrode;

a ~~plurality of~~ scanning lines;

a ~~plurality of data lines, one of the~~ data lines crossing ~~one of~~ the ~~plurality of~~ scanning lines; and

a plurality of transistors disposed correspondingly to intersections between the ~~plurality of~~ data lines and the ~~plurality of~~ scanning lines,

each of the plurality of transistors ~~comprising:~~including

~~———~~a gate electrode~~;~~ and

~~———~~a semiconductor layer, wherein the semiconductor layer comprises a source ~~having a channel~~ region that is connected to the pixel electrode through a contact hole, a drain region that is connected to the data line through a contact hole, ~~and at least one portion extending outside of the~~a channel region disposed under the gate electrode, ~~in a gate width direction perpendicular to a gate length direction,~~ and the channel region having a semiconductor portion protruding out of the channel region and not being covered with the gate electrode ~~that is a direction in which one of the plurality of data lines extends~~.

~~———at least one of a source region and a drain region being separated by an extension of the gate electrode, and the extension extending in the gate length direction outside of the semiconductor region.~~

20. (Amended) the electro-optical device according to claim 1, wherein the semiconductor portions ~~of the plurality of scanning lines form the gate electrodes~~ protruding in a direction in which the scanning line extends.

21. (Amended) ~~A thin film transistor array substrate, comprising:~~

~~———a substrate;~~

~~———a plurality of scanning lines;~~

~~———a plurality of data lines, one of the data lines crossing one of the plurality of scanning lines; and~~

~~———a plurality of transistors disposed correspondingly to intersections between the plurality of data lines and the plurality of scanning lines,~~

~~———each of the plurality of transistors further comprising:~~

~~a gate electrode; and~~

~~a semiconductor having a channel region and at least one portion extending outside of the channel region in a gate-width direction perpendicular to a gate-length direction that is a direction in which one of the plurality of data lines extends,~~

~~the at least one portion and at least one of a source region and a drain region being separated by an extension of the gate electrode~~The electro-optical device according to claim 1, wherein the gate electrode has two parts protruding out of the semiconductor layer, and the source region or the drain region being disposed between the two parts.